METHOD AND APPARATUS FOR TEST CASE EVALUATION USING A CYCLIC REDUNDANCY CHECKER

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to computer architectures and, more particularly, to a method and an apparatus for testing electronic components.

Description of Related Art

Testing of hardware and software generally involves executing a set of instructions and/or commands and comparing the actual results with the expected results. If the actual results match the expected results, the test case was successful. If the actual results do not match the expected results, then the test case failed.

In order to make this determination, however, generally requires capturing large amounts of data, such as a memory dump, transferring the data from the test machine to a host machine, and comparing the data with the expected results. This process is time and resource intensive.

Therefore, there is a need to provide a method and an apparatus to efficiently assist in evaluating test case results.

SUMMARY

The present invention provides an apparatus and a method for testing one or more electrical components. The apparatus and method comprises executing a test on the electrical component and calculating a Cyclic Redundancy Checker (CRC) value for a predetermined portion of memory. The CRC value is compared with an expected CRC value to determine if the test was successful.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a schematic diagram of a typical testing environment that embodies the present invention;

FIGURE 2 is a block diagram illustrating one embodiment of the present invention in which a test platform is used to test an electrical component;

FIGURE 3 is a block diagram illustrating one embodiment of the present invention in which a Cyclic Redundancy Checker (CRC) is placed on a memory card;

FIGURE 4 is a data flow diagram illustrating one embodiment of the present invention in which a CRC function is utilized to determine if an electrical component successfully passed a test; and

FIGURE 5 is a data flow diagram illustrating one embodiment of the present invention in which a CRC function is utilized to determine if a Central Processing Unit (CPU) has successfully passed a boot-up sequence.

DETAILED DESCRIPTION

In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be obvious to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block diagram form in order not to obscure the present invention in unnecessary detail. Additionally, for the most part, details concerning the physical implementation and connectivity of the invention, and the like, have been omitted inasmuch as such details are not considered necessary to obtain a complete understanding of the present invention, and are considered to be within the skills of persons of ordinary skill in the relevant art.

It is further noted that, unless indicated otherwise, all functions described herein may be performed in either hardware or software, or some combination thereof. In a preferred embodiment, however, the functions are implemented in hardware in order to provide the most efficient implementation. Alternatively, the functions may be performed by a processor such as a computer or an electronic data processor in accordance with code such as computer program code, software, and/or integrated circuits that are coded to perform such functions, unless indicated otherwise.

Referring to FIGURE 1 of the drawings, the reference numeral 100 generally designates a test system embodying features of the present invention. The test system 100 generally comprises a host computer 110, such as a Workstation Model 270 manufactured by IBM, Corp., connected to a test platform 112. The host computer 110 is

configured to provide test case information to the test platform 112 and to receive test case results from the test platform 112. A preferred embodiment of the test platform 112 is more particularly described in copending and coassigned U.S. Patent Application Serial Number _____, entitled "Method and System for Testing Electronic Components", which is incorporated by reference herein for all purposes. For purposes of illustration and to clearly describe the present invention, however, a simplified embodiment is discussed below with reference to FIGURE 2.

FIGURE 2 is a block diagram depicting the components that preferably comprise the test platform 112 in accordance with one embodiment of the present invention. Accordingly, the test platform 112 generally comprises one or more devices under test (DUTs), such as CPUs 210, and one or more memories 212. Other components, such as a bus arbiter, I/O chipset, debug connectors, and the like, which may be necessary for the operation of the present invention, are considered well known to a person of ordinary skill in the art, and, therefore, are neither shown nor discussed in greater detail.

The CPUs 210 are configured to perform test cases supplied by the host computer 110 (FIG. 1). The memories 212, preferably Dual In-line Memory Modules (DIMMs), Single In-line Memory Modules (SIMMs), or the like, provide memory for the execution of the test cases and storage of the test case results. In a preferred embodiment, one or more of the memories 212are replaced with a Cyclic Redundancy Checker in a Multiple Instruction Shift Register (CRC-MISR) card, which is discussed in greater detail below with reference to FIGURE 3.

FIGURE 3 is a block diagram depicting the components that preferably comprise a CRC-MISR card in accordance with one embodiment of the present invention. Accordingly, reference numeral 300 generally designates a CRC-MISR card that may be substituted for one or more of the memories 212 (FIG. 2). In the preferred embodiment, the memories 212 are DIMMs, and, therefore, the CRC-MISR card 300 preferably comprises a DIMM-form factor card 310, including a standard DIMM connector 312, configured with a CRC module 314, configuration registers 318, and, optionally, memories 316.

The CRC module 314 determines a CRC value by executing a CRC algorithm on for a range of addresses as specified by the configuration registers 318 and stores the CRC value in the one or more memories 212. Preferably, the host computer 110 (FIG. 1)

configures the configuration registers 318 to specify the address range, *i.e.*, a minimum and maximum address, and an accumulation trigger, such as on read and write transactions, read-only transactions, write-only transactions, and the like. Additionally, it is preferable to allow the host computer 110 to set the configuration registers 318 such that the CRC module 314 is disabled and/or the CRC performs a self-test on a memory segment.

Furthermore, the CRC module 314 is configured to store the result in the one or more memories 316 and/or directly to system memory 212. The result may be transferred to the host computer 110 upon request, at which time the host computer may compare the actual result with the expected result. Alternatively, the host computer 110 may transfer the expected results to the memories 316 and/or 212 and configure the CRC function 314 to compare the actual results to the expected results upon completion of a test. This alternative implementation allows for the ability to only notify and/or send data to the host computer 110 upon a failed test.

CRC algorithms, and their hardware and/or software implementations, are well known in the industry. The use of the CRC algorithms with the present invention, therefore, will be obvious to a person of ordinary skill in the art upon a reading of the present disclosure, and will not be discussed in greater detail except insofar as is necessary to adequately describe the present invention.

FIGURE 4 is a flow chart depicting steps that may be performed by the test system 100 in accordance with one embodiment of the present invention that determines whether a DUT, *i.e.*, CPUs 210 has successfully passed a test case. Processing begins in step 410, wherein a test case is generated and an expected CRC value is determined, preferably by the host computer 110. Processing proceeds to step 412, wherein the host computer 110 initializes the configuration registers 318 on the CRC-MISR 310. As discussed above, it is preferred that the host computer 110 initializes the configuration registers 318 to specify the memory range and the type of transaction. Thereafter, in step 414, the test case is performed on the DUT.

After the test case is performed by the DUT, in step 416 the CRC function 314 determines the actual CRC value from the memories 212 (FIG. 2). In step 418, a determination is made whether the actual CRC value matches the expected CRC value. The determination may be made by either the CRC-MISR card 310 or the host computer

110, as is discussed above. If, in step 418, a determination is made that the actual CRC value matches the expected CRC value, then processing proceeds to step 420, wherein the test is indicated as passed and the memory is released. If, however, in step 418, a determination is made that the actual CRC value does not match the expected CRC value, then processing proceeds to step 422, wherein the test is indicated as failed and results are stored, either in the memory 316 (FIG. 3), the memory 212 (FIG. 2), or the host computer 110.

In step 424, the failed test case is optionally segmented and the expected CRC value recalculated. Segmenting a test case is a method used to narrow the failing condition by taking subsets of the failed test case to determine the specific area in which the DUT fails. After segmenting the test case and recalculating the expected CRC value, processing returns to step 412, wherein the test case is processed.

Alternatively, an expected CRC value may be calculated over a different range of memory. Instead of re-executing the test case or running a different test case, an actual CRC value may be calculated and compared to the expected CRC value. In this manner, further debugging may be performed by inspecting multiple sections of memory after executing a single test case to further determine specific problem areas.

FIGURE 5 is a flow chart depicting steps that may be performed by the test system 100 in accordance with another embodiment of the present invention that determines whether a DUT has successfully passed a boot-up sequence. One particular problem addressed by the present invention is the problem of determining whether a boot up sequence of a DUT such as a CPU has executed properly, and, if not, where in the boot up process the DUT failed. Accordingly, beginning in step 510, intermediate expected CRC values of a passing boot-up sequence are determined, preferably by the host computer 110. Processing proceeds to step 512, wherein the host computer 110 initializes the configuration registers 318 on the CRC-MISR 310. As discussed above, it is preferred that the host computer 110 initialize the configuration registers 318 to specify the memory range and the type of transaction. Thereafter, in step 514, the test case is performed on the DUT.

After the test case is performed by the DUT, in step 516 the CRC function 314 determines the actual CRC value from the memories 212 (FIG. 2). In step 518, a determination is made whether the actual CRC value matches the expected CRC value.

The determination may be made by either the CRC-MISR card 310 or the host computer 110, as is discussed above. If, in step 518, a determination is made that the actual CRC value matches the expected CRC value, then processing proceeds to step 520, wherein the test is indicated as passed and the memory is released. If, however, in step 518, a determination is made that the actual CRC value does not match the expected CRC value, then processing proceeds to step 522, wherein the test is indicated as failed and results are preferably stored, either in the memory 316 (FIG. 3), the memory 212 (FIG. 2), or the host computer 110, for analysis.

In step 524, the failed test case is optionally segmented and the expected CRC value recalculated, and processing returns to step 512, wherein the segmented test case is processed.

It should be noted that the foregoing disclosure discusses the invention in terms of the preferred embodiment in which the host computer is an external host computer configured to control the execution of test cases and the like. The invention, however, is equally applicable to the situation in which the host computer does not exist and the CRC-MISR cards are inserted into a stand-alone system, such as replacing one or more memory cards of a personal computer (PC) with one or more CRC-MISR cards. In this situation, the CPU of the stand-alone system preferably performs the functions of the host computer and application programs may be written to test various aspects of the hardware/software design, the results of which may be determined as described above. The use of the present invention in such an environment is considered to be within the skills of a person of ordinary skill in the art upon a reading of the present disclosure.

It is understood that the present invention can take many forms and embodiments. Accordingly, several variations may be made in the foregoing without departing from the spirit or the scope of the invention. For example, additional monitors may be utilized to monitor bus traffic and/or detect errors in specific cycles.

Having thus described the present invention by reference to certain of its preferred embodiments, it is noted that the embodiments disclosed are illustrative rather than limiting in nature and that a wide range of variations, modifications, changes, and substitutions are contemplated in the foregoing disclosure and, in some instances, some features of the present invention may be employed without a corresponding use of the other features. Many such variations and modifications may be considered obvious and

desirable by those skilled in the art based upon a review of the foregoing description of preferred embodiments. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.